Trainee's Project Report

Job Code	PH1623
Department	PH
Discipline	Electronics Engineering
Supervisor	RODRIGUES SIMOES MOREIR

Description

Design of communications integrated circuits
The candidate will work at CERN in the micro-electronics section for a period of two years. He/she will be involved in the development of a high speed data communications ASIC that will be used in the future SLHC experiments. The engineer will use a mix of full-custom and standard cell design techniques and will be involved on the design of variety of circuits such as phase-locked loops, serializers, clock recover circuits, high speed line drivers and on the design of digital logic. Additionally, the engineer will be also involved on evaluation testing of the ASIC.

Special Requirements

A university degree in electronics engineering is required. The candidate should have understanding of analogue electronics and communication circuits. The candidate should be acquainted with the use of CAD tools for full-custom ASIC design. Knowledge of Verilog or VHDL hardware programming languages would be considered as an asset.

Training Value

The candidate will be integrated in an electronics engineering group for which the main activity is ASIC design. The candidate will develop skills on the design of analogue and communications circuit, will become proficient on the use of full-custom and standard cell design CAD tools and will learn and use equipment for ASIC characterization and evaluation testing.